

**Listing of the Claims:**

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1        1 (Currently Amended). A computer firmware program updating system  
2        having a communication function comprising:  
3                a first processor which operates by referring to a firmware program  
4        stored ~~therein~~ in a flash ROM; and  
5                a second processor which monitors an operation of said first  
6        processor and executes update of said firmware program by using said  
7        communication function with an external unit, and executes an update  
8        control of said program when a fault of said first processor is detected.

1        2 (Previously Presented). The program updating system having the  
2        communication function according to claim 1,  
3                wherein said second processor transmits a reset signal to said first  
4        processor for every predetermined number of cycles, and monitors a  
5        response pulse which is transmitted from said first processor in response to  
6        said reset signal, and transmits a compulsory reset signal to said first  
7        processor when said response pulse can not be detected within a  
8        predetermined period.

1        3 (Previously Presented). The program updating system having the  
2        communication function according to claim 2, further comprising:  
3                an activation pulse generating circuit which generates an activation  
4        pulse to activate said second processor,  
5                wherein said second processor starts transmitting said reset signal  
6        in response to said activation pulse outputted from said activation pulse  
7        generating circuit.

1        4 (Currently Amended). The program updating system having the  
2        communication function according to claim 3, further comprising:

3 a buffer which transiently stores ~~said~~ a program to be used for  
4 executing said firmware program update ~~control~~, wherein said second  
5 processor transfers said program stored in said buffer to said first processor  
6 for writing into said flash ROM, after an operation of storing said program  
7 in said buffer is completed.

1 5 (Currently Amended). The program updating system having the  
2 communication function according to claim 1, further comprising:  
3 an activation pulse generating circuit which generates an activation  
4 pulse to activate said second processor,  
5 wherein said second processor starts transmitting ~~said~~ a reset signal  
6 to said first processor in response to said activation pulse outputted from  
7 said activation pulse generating circuit.

1 6 (Currently Amended). The program updating system having the  
2 communication function according to claim 5, further comprising:  
3 a buffer which transiently stores ~~said~~ a program for executing said  
4 firmware program update ~~control~~, wherein said second processor transfers  
5 said program stored in said buffer to said first processor for writing into  
6 said flash ROM, after an operation of storing said program to said buffer is  
7 completed.

1 7 (Currently Amended). The program updating system having the  
2 communication function according to claim 1, further comprising:  
3 a buffer which transiently stores ~~said~~ a program for executing said  
4 firmware program update ~~control~~, wherein said second processor transfers  
5 said program stored in said buffer to said first processor for writing into  
6 said flash ROM, after an operation of storing said program to said buffer is  
7 completed.

1 8 (Original). The program updating system having the communication  
2 function according to claim 2, further comprising:

3 an activation monitoring circuit which generates an activation pulse  
4 to activate said second processor and monitors transmission of an  
5 activation response pulse which is outputted from said second processor in  
6 response to said activation pulse,

7 wherein said activation monitoring circuit transmits a compulsory  
8 reset signal to said second processor when said activation response pulse  
9 can not be detected within the predetermined period.

1 9 (Currently Amended). The program updating system having the  
2 communication function according to claim 8, further comprising:

3 a buffer which transiently stores ~~said~~ a program for executing said  
4 firmware program update ~~control~~, wherein said second processor transfers  
5 said program stored in said buffer to said first processor for writing into  
6 said flash ROM, after an operation of storing said program to said buffer is  
7 completed.

1 10 (Currently Amended). The program updating system having the  
2 communication function according to claim 1, further comprising:

3 an activation monitoring circuit which generates an activation pulse  
4 to activate said second processor and monitors transmission of an  
5 activation response pulse outputted from said second processor in response  
6 to said activation pulse,

7 wherein said activation monitoring circuit transmits a compulsory  
8 reset signal to said second processor when said activation response pulse  
9 can not be detected within ~~the~~ a predetermined period.

1 11 (Currently Amended). The program updating system having the  
2 communication function according to claim 10, further comprising:

3 a buffer which transiently stores ~~said~~ a program for executing said  
4 firmware program update ~~control~~, wherein said second processor transfers  
5 said program stored in said buffer to said first processor for writing into  
6 said flash ROM, after an operation of storing said program to said buffer is

7 completed.

1 12. (Currently Amended) A computer firmware program updating method  
2 using a communication function, comprising:

3 providing a first processor which operates by referring to a  
4 firmware program stored therein in a flash ROM and a second processor;  
5 transmitting a reset pulse from said second processor to said first  
6 processor;

7 transmitting a response pulse from said first processor to said  
8 second processor in response to said reset signal which is outputted from  
9 said second processor; and

10 transmitting a compulsory reset signal from said second processor  
11 to said first processor to stop an operation of said first processor when said  
12 response pulse can not be detected within a predetermined period.

1 13 (Currently Amended). The program updating method using the  
2 communication function according to claim 12, ~~wherein~~ further  
3 comprising:

4 transferring by said second processor ~~transfers said a~~ program  
5 obtained by using said communication function to said first processor for  
6 writing into said flash ROM, during a stop of said first processor.

1 14 (Currently Amended). The program updating method using the  
2 communication function according to claim 13, further comprising:

3 providing an activation control circuit which controls activation  
4 and a stop of said second processor,

5 ~~wherein~~ transmitting by said second processor ~~transmits~~ an  
6 activation response pulse to said activation control circuit for every  
7 predetermined number of cycles, and

8 executing by said activation control circuit ~~executes~~ a stop control  
9 of said second processor, when said activation response pulse can not be  
10 detected within a predetermined period.

1        15 (Currently Amended). The program updating method using the  
2        communication function according to claim 12, further comprising:  
3            providing an activation control circuit which controls activation  
4        and a stop of said second processor, ~~wherein:~~  
5            transmitting by said second processor ~~transmits~~ an activation  
6        response pulse to said activation control circuit for every predetermined  
7        cycles; and  
8            executing by said activation control circuit ~~executes~~ a stop control  
9        of said second processor, when said activation response pulse can not be  
10       detected within a predetermined period.